

Remarks:

Reconsideration of the application is requested.

Claims 1-18 are now in the application. Claims 1-13 have been amended. Claims 5-6, 8, and 14-16 have been withdrawn from consideration. Claims 17 and 18 have been added.

Support for the subject-matter of newly added claims 17-18 can be found in Fig. 1 of the instant application and the corresponding disclosure.

In the last paragraph on page 2 of the above-identified Office action, the drawings have has been objected for not showing a reference signal. The drawings have been appropriately amended.

In the first paragraph on page 3 of the Office action, the disclosure has been objected to because of one informality. The Examiner's comments have been noted and the appropriate corrections have been made to the disclosure on page 4 of the instant application.

In the third paragraph on page 3 of the Office action, claims 1-4, 7, and 9-13 have been rejected as being indefinite under 35 U.S.C. § 112, first paragraph.

More specifically, the Examiner has stated that "[a]n integrated circuit as enabled by specification must have a signal selecting device using a reference signal for selectively testing a signals from a plurality of circuit points." The Examiner's comments have been considered and claim 1 has been amended to recite "at least one multiplexer".

Not in claim

In the fourth paragraph on page 3 of the Office action, claims 1-4, 7, and 9-12 have been rejected as containing subject matter which was not sufficiently described in the specification under 35 U.S.C. § 112, first paragraph. More specifically, the Examiner has stated that "[c]laim 1 recites selectively testing any of the various electrical signals provided by a plurality of circuit points ... using a reference signal." Applicants believe that there is sufficient disclosure. The appropriate correction has been made to the specification to clarify the specification.

In the third paragraph on page 4 of the Office action, claims 2-3, 7, 9, and 10-13 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph. More specifically, the Examiner has stated that there is insufficient antecedent basis for the limitation "at least one external test connecting contact point" in claims 2-3, 7, 9, and 10-13. The

Examiner's comments have been noted and the appropriate corrections have been made to claims 2-13.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, first and second paragraphs. Should the Examiner find any further objectionable items, Counsel would appreciate a telephone call during which the matter may be resolved. The above-noted changes to the claims are provided solely for the purpose of satisfying formal requirements, clarification, or are made solely for cosmetic reasons to clarify the claims. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claims for any reason related to the statutory requirements for a patent.

In the second paragraph on page 5 of the Office action, claims 1-4 and 10-13 have been rejected as being anticipated by Quinn (US 3,801,910) under 35 U.S.C. § 102.

In the fifth paragraph on page 7 of the Office action, the Examiner stated that "Quinn discloses all the essential elements of the claimed invention except for a ... multiplexing circuit". Consequently, it is believed that adding the feature "multiplexer" to claim 1 has overcome the rejection of claim 1 as being anticipated by Quinn.

Now
True

In the fourth paragraph on page 7 of the Office action, claims 7 and 9 have been rejected as being obvious over *Quinn* in view of *Du Chene et al.* (US 4,982,403) under 35 U.S.C. § 103.

As will be explained below, it is believed that claims 7 and 9 were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome *Quinn* in view of *Du Chene et al.*.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 (similarly claim 17) as amended calls for, inter alia:

a plurality of circuit points being not externally accessible, providing various electrical signals of the integrated circuit component to be measured or analyzed;

at least one connecting contact point externally; and

a multiplexer having an output connected to said at least one connecting contact point and having a plurality of inputs, each one of said plurality of inputs being connected to a respective one of said plurality of circuit points.

Quinn discloses a structure for selectively externally accessing mechanically difficult to access circuit nodes using photo-responsive conductors in an integrated circuit. As

stated above, *Quinn* does not disclose a multiplexing circuit. The Examiner therefore applies the secondary reference *Du Chene et al.* for disclosing "a time-controlled multiplexing circuit". The Examiner then states that "[i]t would have been obvious ... to modify the integrated circuit component of *Quinn* and substitute ... multiplexing circuit of *Chene* for a laser source".

In order to establish a *prima facie* case of obviousness by modifying or combining reference teachings, MPEP § 2143 requires that:

- there must be ***some suggestion or motivation*** to combine the references in the prior art;
- there must be a ***reasonable expectation of success*** to be found in the prior art; and
- the prior art references must teach or suggest all the claim limitations.

Each externally accessible contact point in *Quinn* only contacts one particular internal circuit point. Simply replacing the photoconductive device(s) with a multiplexing circuit would not lead to the recited device since the multiplexer has a "plurality of inputs, each one of said plurality of inputs being connected to a respective one of said plurality of circuit points". Accordingly, it is believed that there is no suggestion or motivation with a reasonable expectation of success in the prior art for

combining *Quinn* with *Du Chene et al.* as performed by the Examiner.

It is accordingly believed to be clear that *Quinn* in view of *Du Chene et al.* do not suggest the features of claims 1 and 17. Claims 1 and 17 are, therefore, believed to be patentable over the art and because claims 2-13 are ultimately dependent on claim 1 and claim 18 is dependent upon claim 17, they are believed to be patentable as well.

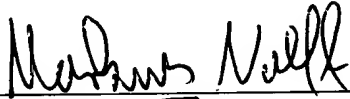
In view of the foregoing, reconsideration and allowance of claims 1-13 and 17-18 are solicited.

If an extension of time is required, petition for extension is herewith made.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Applic. No. : 09/740,634

Respectfully submitted,



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Version with markings to show changes made:

Page 4, lines 12-22, --

The use of external test connecting contact points allow internal chip signals to be seen and the timing to be determined accurately. For this purpose, a reference signal is selectively applied to one of the external test connecting contact points such that it can be passed on via a route within the component to [one of the external test connecting contact points from] a circuit point which is not externally accessible[, and in that signals]. Signals which are to be measured or are to be analyzed can in each case be selectively applied such that they can be passed on ^{not shown} via routes within the component from circuit points which are not externally accessible to the other test connecting contact points [from circuit points which are not externally accessible]. --

Claim 1 (amended). An integrated circuit component, comprising:

a plurality of circuit points not being [not] externally accessible, providing various electrical signals of the integrated circuit component to be measured or analyzed; [and] at least one connecting contact point being externally accessible [for selectively testing any one of the various

electrical signals, said at least one connecting contact point being connected via routes within the integrated circuit component to said plurality of circuit points being not externally accessible]; and

a multiplexer having an output connected to said at least one connecting contact point and having a plurality of inputs, each one of said plurality of inputs being connected to a respective one of said plurality of circuit points.

Claim 2 (amended). The integrated circuit according to claim 1, wherein:

said at least one [external test] connecting contact point is one of a plurality of [external test] connecting contact points;

a reference signal is selectively applied to one of said plurality of connecting contact points and passed on via a route within the integrated circuit component to one [of said plurality of external test connecting contact points from one] of said plurality of circuit points that are not externally accessible; and

said signals to be measured or analyzed can be selectively [applied to be] passed on via routes within the integrated circuit component from said plurality of circuit points that are not externally accessible to said plurality of [external

test] connecting contact points other than said one of said plurality of [external test] connecting contact points.

Claim 3 (amended). The integrated circuit according to claim 2, wherein said plurality of [external test] connecting contact points is exactly two [external test] connecting contact points.

Claim 4 (amended). The integrated circuit according to claim 1, wherein:

said electrical signals are internal chip signals in the integrated circuit component; and

reference signals and said electrical signals can be selectively passed on to said at least one [external test] connecting contact point.

Claim 5 (amended). The integrated circuit according to claim 1, comprising a package and wherein:

said plurality of connecting contact points define a plurality of inaccessible contact points disposed on said package;

said electrical signals at said plurality of circuit points that are not externally accessible are present at said plurality of inaccessible contact points;

said electrical signals and reference signals are selectively passed on to said at least one [external test] connecting contact point; and

said at least one [external test] connecting contact point is formed by at least one of said plurality of inaccessible contact points.

Claim 6 (amended). The integrated circuit according to claim 5, wherein:

said package is a ball grid array package having a lower face;

said plurality of inaccessible contact points are located on said lower face of said package and are thus concealed between said package and a system board on which [the] said package is fitted; and

said at least one [external test] connecting contact point is electrically conductively connected to a corresponding number of metallic test points on the system board.

Claim 7 (amended). The integrated circuit according to claim [1] 3, [wherein a time-controlled] further comprising a second multiplexing circuit [is provided for selectively passing on the electrical signals to said at least one external test connecting contact point].

Claim 8 (amended). The integrated circuit according to claim [7] 1, wherein:

said [time-controlled] multiplexing circuit is time-controlled [has inputs and an output] and is provided in the integrated circuit component [which is] surrounded by a ball grid array package[;

said plurality of contact points which are not used as connecting contact points are electrically conductively connected to said inputs of said multiplexing circuit;

said output of said time-controlled multiplexing circuit is electrically conductively connected to one of said plurality of contact points in the package which forms said at least one connecting contact point].

Claim 9 (amended). The integrated circuit according to claim 7, wherein said multiplexing circuit is programmably controlled to predetermine selective passing on of the electrical signals to said at least one [external test] connecting contact point.

Claim 10 (amended). The integrated circuit according to claim 1, wherein said at least one [external test] connecting contact point can be selectively used in an opposite operating

direction for inputting signals to said plurality of circuit points that are not externally accessible.

Claim 11 (amended). The integrated circuit according to claim 1, wherein said at least one [external test] connecting contact point is connected to a component tester for analyzing the electrical signals at, at least some of said plurality of circuit points.

Claim 12 (amended). The integrated circuit according to claim 1, wherein said at least one [external test] connecting contact point is connected to a system and an application of said system analyzes the electrical signals at, at least some of said plurality of circuit points.

Claim 13 (amended). The integrated circuit according to claim 1, wherein said at least one [external test] connecting contact point is used for analyzing a system in which said integrated circuit is used.